Lawrence Tang

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Education

Carnegie Mellon University | Pittsburgh, PA *2020 - Present*
Ph.D. Candidate in Electrical and Computer Engineering
Advisors: Prof. Franz Franchetti & Prof. Ken Mai

Carnegie Mellon University | Pittsburgh, PA *2020 - 2022*
M.S. Electrical and Computer Engineering
GPA: 4.00

Cornell University | Ithaca, NY *2016 - 2020*
B.S. Electrical and Computer Engineering
GPA: 3.99

Awards and Honors

Apple PhD Fellowship in Integrated Systems *2023*
Carnegie Institute of Technology Dean's Fellow *2020*
Cornell Engineering Learning Initiatives Undergraduate Research Grant *2018 and 2019*
Tau Beta Pi Engineering Honor Society *2018*
IEEE-Eta Kappa Nu *2018*

Research Experience

Carnegie Mellon University | Pittsburgh, PA *Aug '20 – Present*
Graduate Student Researcher, Advisors: Prof. Franz Franchetti and Prof. Ken Mai
- Working on new design paradigms for hardware accelerators in FFT based applications
- Developing a flexible architecture to support a variety of FFT-based workloads and to enable end-to-end system level integration in an SoC from user code to hardware implementation
- Designed microarchitecture and physical implementation of prototype FFT ASIC testchips in a 28nm process; built custom PCB and evaluated testchip
- Looking at applications in large integer multiplication, machine learning, and HPC scientific workloads

VLSI Information Processing Group | Cornell University *Jun '17 – Aug '20*
Undergraduate Research Assistant, Advisor: Prof. Christoph Studer
- Implemented hardware efficient algorithms for wireless localization using channel state information (CSI) with the approximate nearest neighbor search and Locality-Sensitive Hashing (LSH) methods
- Designed new neural network based methods for unsupervised localization in Hamming space using CSI

Professional Experience

Apple | Austin, TX *May '23 – Aug '23*
Physical Design CAD Intern
- Analysis of routines for repeater insertion in the top-level PNR flow
- Explored optimizations to improve the quality and efficiency of top-level buffer insertion

MITRE | Bedford, MA *May '18 – Aug '19*
Intern in Positioning, Navigation, and Timing
- Quantitatively analyzed GNSS navigational measurements and errors to assess potential utility of future GNSS satellite capabilities
- Analyzed GNSS signal processing techniques used for adaptive antenna arrays and GPS signals through modeling, simulation, and experimental RF hardware testing

Publications

A. Shah, **L. Tang**, P. H. Chou, Y. Y. Zheng, Z. Ge and B. Raj, "An Approach to Ontological Learning from Weak Labels," IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP), June 2023

L. Tang, S. Chen, K. Harisrikanth, G. Xu, K. Mai and F. Franchetti, "A High Throughput Hardware Accelerator for FFTW Codelets: A First Look," IEEE High Performance Extreme Computing Conference (HPEC), Sept. 2022

L. Tang, R. Ghods, C. Studer, "Reducing the Complexity of Fingerprinting-Based Positioning using Locality-Sensitive Hashing," Asilomar Conference on Signals, Systems, and Computers, Nov. 2019

Presentations/Preprints

L. Tang, P.H. Chou, Y.Y. Zheng, Z. Ge, A. Shah, B. Raj, "Ontological Learning from Weak Labels", arXiv preprint arXiv:2203.02483

Z. Gong, N. Zhu, M. Ngaw, J. Rivera, **L. Tang**, E. Tang, H. Mankad, F. Franchetti, "Interval Arithmetic-based FFT for Large Integer Multiplication", IEEE High Performance Extreme Computing Conference (HPEC), 2022, Poster with extended abstract

J. Nguyen, M. Cai, Z. Zuo, **L. Tang**, K. Mai, F. Franchetti, "LIMA: Hardware for FFT based Large Integer Multiplication", IEEE High Performance Extreme Computing Conference (HPEC), 2022, Extended abstract

L. Tang, R. Ghods, C. Studer, "Fingerprinting-Based Positioning using Locality-Sensitive Hashing," ELI Undergraduate Research Poster Session, Ithaca, NY, May 2019

Projects

A High Throughput FFT Accelerator for FFTW Codelets | Carnegie Mellon University *Spring '21*

- Designed and implemented an 8 point FFT ASIC prototype testchip in a TSMC 28nm process
- Fully unrolled, deeply pipelined design for high throughput running at ∼260 MHz clock under nominal conditions
- The first silicon verified testchip co-designed using SPIRAL generated hardware

VLSI Implementation of 16-bit CORDIC | Cornell University *Spring '19*

- Full-custom design of schematics and layout to implement a 16-bit pipelined rotation CORDIC using Cadence Virtuoso; Testing and verification performed using MATLAB and Python scripts
- Wrote equivalent RTL models to the custom CORDIC design to compare post-synthesis area and timing metrics to our custom layout

Teaching Experience

Graduate Teaching Assistant | Carnegie Mellon University

- 18-725: Advanced Digital Integrated Circuit Design *Spring 2023, 2024*
- 18-622: Digital Integrated Circuit Design *Fall 2022, 2023*

Undergraduate Teaching Assistant | Cornell University

- ECE 3150: Introduction to Microelectronics *Spring 2020*
- CS 4780: Machine Learning for Intelligent Systems *Fall 2019*
- ECE 2300: Digital Logic and Computer Organization *Spring 2019*

Selected Coursework

Advanced Digital Integrated Circuit Design • Complex Digital ASIC Design • Digital VLSI Design • Reconfigurable Computing • Digital System Testing and Testable Design • Analog Integrated Circuit Design • Computer Architecture • Wireless Communications • Numerical Analysis • Digital Signal and Image Processing • Deep Learning • Machine Learning for Intelligent Systems • Data and Network Science

Skills

Software: Python, C, C++, TCL, MATLAB, PyTorch, Keras, Java

Hardware: SystemVerilog, Verilog, Cadence